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Electrical Field Engineering of a Metal Capping Layer for Enhanced Oxide Thin-Film Transistor Performance

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Abstract: Amorphous silicon zinc tin oxide (a-SZTO) thin-film transistors (TFTs) were fabricated and systematically investigated by varying the oxygen flow parameter (OFP) during channel deposition and the metal capping (MC) width on the device structure. The a-SZTO active layer was deposited by RF sputtering, while Ti/Al was used as the source/drain electrode and metal capping layer. The effects of OFP and MC width on the electrical performance of the TFTs were analyzed through current-voltage measurements, including field-effect mobility (μFE), threshold voltage (V_{th}), subthreshold swing (SS) and total trap density (N_T). For uncapped devices, increasing the OFP from 0 to 10 sccm reduced μ_{FE} from 14.53 to 8.85 cm^2/Vs and shifted V_{th} from 3.68 to 7.31 V, while SS improved from 0.78 to 0.66 V/decade and N_T decreased from 3.41 to 2.09 × 10^{12} $cm^{-2}eV^{-1}$. These results indicate that higher oxygen incorporation suppresses oxygen-vacancy-related donor states and reduces trap density but also lowers the free carrier concentration in the channel. In contrast, the introduction of the Ti/Al metal capping layer increased μ_{FE} and shifted V_{th} in the negative direction for all OFP conditions, confirming enhanced electron injection from the capping layer into the a-SZTO channel. At an OFP of 10 sccm, μ_{FE} increased from 8.85 to 11.02 cm^2/Vs and V_{th} shifted from 7.31 to -1.18 V as the MC width increased from 0 to 40 μm. The transfer-characteristic trends were also consistent with the output characteristics, further verifying that OFP and MC width strongly influence carrier concentration and channel conductivity.

Keywords: Amorphouse Oxide, SZTO, TFT, Thin-Film Transistor, Metal Capping Layer

1. Introduction

Amorphous silicon zinc tin oxide (a-SZTO) has attracted significant attention from both academia and industry as an active channel material because of its promising electrical and material properties, including high field-effect mobility (μFE), a high on/off current (Ion/off) ratio, low-temperature process compatibility, and good large-area uniformity. A μFE value exceeding 20 cm2/Vs is generally considered necessary for next-generation flat panel displays (FPDs), particularly for demanding applications such as AMOLED panels, 8K ultra-high-resolution displays with high frame rates, and large-area display technologies. In this regard, a-SZTO is regarded as a highly promising channel material for achieving the performance requirements of future FPD backplane systems [1-3].

Although a-SZTO offers clear advantages, especially in terms of high mobility and low-temperature fabrication, it has not yet been widely adopted as a mainstream backplane material in the display industry because of concerns related to electrical instability. The electrical performance of a-SZTO thin-film transistors (TFTs) has been extensively studied experimentally and theoretically by tuning the relative composition of Si, Zn, and Sn, since the balance among these constituent metals strongly influences carrier transport, defect formation, and threshold voltage behavior [4-7]. Therefore, compositional engineering remains one of the key strategies for improving device performance and reliability.

Several process parameters have also been explored to improve the stability of a-SZTO TFTs, including channel thickness, silicon content, thermal annealing, and related post-deposition treatments [8-16]. In our previous work, X-ray photoelectron spectroscopy (XPS) analysis was employed to correlate Vth variation with the oxygen chemical states in the film, indicating that the Vth shift was reduced when the oxygen 1s peak associated with higher binding energy increased with increasing oxygen flow pressure (OFP) during deposition [1-3, 16]. However, increasing the OFP during deposition also substantially affects the BTS response by altering the amount of incorporated oxygen and the defect chemistry within the AOS layer [17-22, 23]. Thus, OFP must be carefully optimized because excessive oxygen incorporation may suppress

oxygen-vacancy-related defects while simultaneously modifying carrier concentration, trap formation, and bias stress behavior.

In the present study, the OFP was varied at 0, 5, and 10 sccm, and the effect of different metal capping widths (0, 20, 30, and 40 μm) on device performance was systematically investigated in a-SZTO TFT structures. The influence of these parameters on key electrical properties, including μFE, subthreshold swing (SS), total trap density (N_T), V_{th}, and PBTS stability, was analyzed through current-voltage (I-V) measurements. In general, adjusting the OFP during channel deposition is an effective method for suppressing VO-related defects and improving film densification, which can enhance the interfacial and bulk quality of the semiconductor layer. In addition, the introduction of metal capping is expected to play an important role in improving charge transport characteristics. The metal capping layer can promote more efficient carrier conduction, reduce access resistance in the channel region, and support a more conductive pathway, which may lead to improved mobility and better overall device operation [2]. At the same time, the width of the metal capping can influence the extent of this effect, making it an important structural parameter for optimizing TFT performance and stability. Therefore, the combined control of OFP and metal capping geometry provides an effective route for understanding and improving the electrical characteristics and PBTS reliability of a-SZTO TFTs.

The novelty of this work lies in the combined process-structure engineering of a-SZTO TFTs through oxygen flow modulation during channel deposition and width-controlled Ti/Al metal capping. This study demonstrates that oxygen flow primarily governs defect suppression and trap-state reduction, whereas metal capping width strongly influences electron injection and threshold voltage control. By systematically correlating these factors with mobility, subthreshold swing, trap density, hysteresis, and PBTS behavior, the work provides a distinct and practical framework for optimizing a-SZTO TFTs for next-generation display applications.

2. Experimental details

2.1. Fabrication of a-SZTO TFTs

The conventional a-SZTO thin-film transistors (TFTs) were fabricated in a bottom-gate, top-contact drain/source configuration, as illustrated in Figure 1(a). A heavily boron-doped silicon wafer (p^{++}-Si) was used as the gate electrode, and a 100 nm thick SiO_2 layer was thermally grown on the p^{++}-Si substrate to serve as the gate insulator (GI). Prior to film deposition, the substrates were sequentially cleaned in acetone, methanol, and deionized water using ultrasonication for 10 min in each solvent.

Following the cleaning process, a-SZTO thin films were deposited on the SiO_2 gate insulator by RF sputtering. The deposition parameters used for channel formation are summarized in Table 1. For the channel target, a ceramic mixture composed of high-purity (99.99%) SiO_2, SnO_2, and ZnO powders was prepared, where approximately 0.5 wt. % Si was incorporated into ZTO with a Zn:Sn ratio of 65:35. The active channel region was defined by conventional photolithography, followed by wet etching. The channel width (W) and length (L) were fixed at 250 μm and 50 μm, respectively.

The channel region was defined by conventional photolithography followed by a wet-etching process. The channel width (W) and length (L) were fixed at 250 μm and 50 μm, respectively.

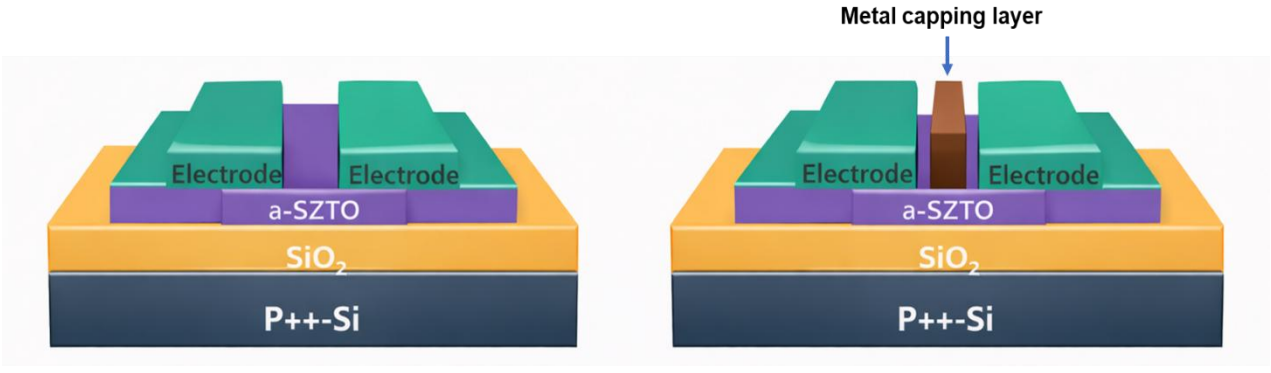

Figure 1. Schematics of **(a)** conventional and **(b)** metal capped TFT structures

Table 1. Deposition conditions for the a-SZTO channel layer

Deposition parameter	Condition
Sputtering power	30 W
Deposition pressure	6 mTorr
Deposition temperature	Room temperature
Argon (Ar) flow rate	40 sccm
Oxygen flow pressure (OFP)	0, 5, and 10 sccm
MC width	0, 20, 30, and 40μm
Deposition time	6 min
Post-annealing temperature	500 °C
Post-annealing time	120 min

To complete the TFT device structure, the source and drain electrodes, together with the metal capping layers, were formed using Ti (10 nm)/Al (40 nm) deposition by electron-beam evaporation and thermal evaporation, followed by a lift-off process. Metal capping (MC) layers widths of 0, 20, 30, and 40 μm were employed to examine their influence on device behavior. The schematic structure of the fabricated a-SZTO TFTs is presented in Figure 1(b).

2.2. Characterization of a-SZTO TFTs

The electrical characteristics of the fabricated TFTs were examined through current-voltage (I-V) measurements using semiconductor parameter analyzers (EL 423, ELECS Co. and 4145B, HP) under dark conditions. The transfer curves were obtained by sweeping the gate voltage from -20 to 40 V while maintaining the drain voltage at 5.1 V.

3. Results and Discussion

Figure 2 shows the transfer characteristics of the fabricated TFTs with different metal capping (MC) widths of 0, 10, 20, and 30 μm under oxygen flow conditions of 0, 5, and 10 sccm at a fixed drain voltage of VD = 5.1 V. In general, amorphous oxide semiconductor TFTs are highly sensitive to gate-bias-induced charge trapping, which can lead to noticeable changes in the threshold voltage (V_{th}). For the devices without metal capping, the transfer curves gradually shift toward the positive gate-voltage region as the oxygen flow rate increases. This behaviour can be attributed to the suppression of oxygen-vacancy-related defects and the reduction of free carrier concentration in the channel, which requires a higher gate bias to turn on the device. In other words, the increased oxygen supply during deposition reduces oxygen-related donor states, thereby shifting V_{th} in the positive direction [15]. In contrast, when the metal capping layer is introduced, the transfer curves shift toward the negative gate-voltage region as the capping width increases. This negative shift is mainly associated with an electron-injection effect induced by the Ti/Al capping layer. Because of the work-function difference between the metal capping layer and the a-SZTO channel, electrons are transferred from the capping layer into the conduction band of the semiconductor. As a result, the carrier concentration in the channel increases, making the device turn on more easily at lower gate voltages. This explains the progressive negative movement of V_{th} with increasing capping width [23, 2, 16].

The μ_{FE} was calculated from the following equation (1) [16, 24]

$$\mu_{FE} = \frac{L \times g_m}{W \times C_{ox} \times V_D} \quad (1)$$

Where g_m is the transconductance and C_{ox} is the gate-insulator capacitance per unit area. Previous studies have shown that suppression of oxygen vacancies (V_O) can reduce the electrical performance of oxide TFTs, often leading to a decrease in μ_{FE} [25, 26].

The total trap density (N_T) was estimated from Eq. (2) [27]:

$$N_T = \left[\frac{SS\log(e)}{kT/q} - 1\right]\frac{C_{ox}}{q} \quad (2)$$

where k, T, q, and $e$represent the Boltzmann constant, absolute temperature, electron charge, and the base of the natural logarithm, respectively. Another important electrical parameter of TFTs is the SS, which was extracted from the linear region of the transfer curve using $SS = \partial V_g / \partial \log I_D$ in units of V/decade.

Table 2. The electrical parameters of a-SZTO TFTs extracted from I-V characteristics for different OFP with no capping layers

OFP (sccm)	MC width (μm)	μ_{FE} cm^2/Vs	SS V/decade	V_{th} (V)	N_T $x10^{12}(cm^{-2}eV^{-1})$
0	0	14.53	0.78	3.68	3.41
	20	15.56	0.80	3.12	3.61
	30	16.81	0.81	2.31	3.69
	40	17.06	0.79	1.51	3.78
5	0	9.56	0.72	5.12	2.61
	20	10.51	0.77	4.20	2.66
	30	11.21	0.86	3.82	2.89
	40	11.98	0.91	1.01	3.15
10	0	8.85	0.66	7.31	2.09
	20	10.16	0.78	2.35	2.16
	30	10.58	0.86	0.18	3.42
	40	11.02	0.98	-1.18	4.12

In general, SS reflects the extent of trap states present in the device, and therefore serves as an indicator of N_T, which includes both the bulk trap density (N_{bulk}) in the a-SZTO film and the interface trap density (N_{it}) at or near the a-SZTO/SiO_2 interface.

For the uncapped TFTs, increasing the OFP from 0 to 10 sccm causes a gradual reduction in μ_{FE} from 14.53 to 8.85 cm^2/Vs (Table 2). This decrease suggests that higher oxygen incorporation suppresses oxygen-vacancy-related donor states, thereby lowering the free electron concentration in the a-SZTO channel. At the same time, the V_{th} shifts positively from 3.68 to 7.31 V, indicating that a larger gate bias is required to induce channel conduction under oxygen-rich conditions. In contrast, the subthreshold swing (SS) improves from 0.78 to 0.66 V/decade, while the total trap density (N_T) decreases from 3.41 × 10^{12} to 2.09 × 10^{12} $cm^{-2}eV^{-1}$. These results imply that increasing OFP helps reduce trap-related defects and improves the switching quality of the device, even though it reduces carrier transport capability.

When the metal capping layer is introduced, the electrical behavior changes significantly. For all OFP conditions, increasing the MC width generally enhances μ_{FE} and shifts V_{th} toward the negative direction (Table 2). At OFP = 0 sccm, μ_{FE} increases from 14.53 to 17.06 cm^2/Vs as the MC width increases from 0 to 40 μm, while V_{th} decreases from 3.68 to 1.51 V. A similar trend is observed at 5 sccm, where μ_{FE} rises from 9.56 to 11.98 cm_2/Vs and V_{th} shifts from 5.12 to 1.01 V. At 10 sccm, the effect becomes much stronger, with μ_{FE} increasing from 8.85 to 11.02 cm^2/Vs and V_{th} moving dramatically from 7.31 to -1.18 V. This strong negative shift in V_{th} confirms that the metal capping layer promotes electron injection into the a-SZTO channel, which increases channel conductivity and lowers the gate voltage required for turn-on.

The effect becomes more pronounced as the capping width increases, indicating that a larger capping area strengthens the carrier donation effect. However, the behavior of SS and NT with increasing MC width is different from that of μ_{FE} and V_{th}. Although the capping layer improves conductivity, it generally causes SS to increase and N_T to rise, especially at higher OFP and wider capping widths. For example, at 10 sccm, SS increases from 0.66 to 0.98 V/decade, and NT rises from 2.09 to 4.12 × 10^{12} $cm^{-2}eV^{-1}$ as the MC width increases from 0 to 40 μm.

This suggests that while the capping layer improves carrier injection and mobility, it may also introduce additional interface-related defects or increase trap-assisted charge interaction near the capped region. Thus, the metal capping layer provides a trade-off: it enhances carrier transport and reduces V_{th}, but excessive capping width may degrade switching sharpness and increase trap density.

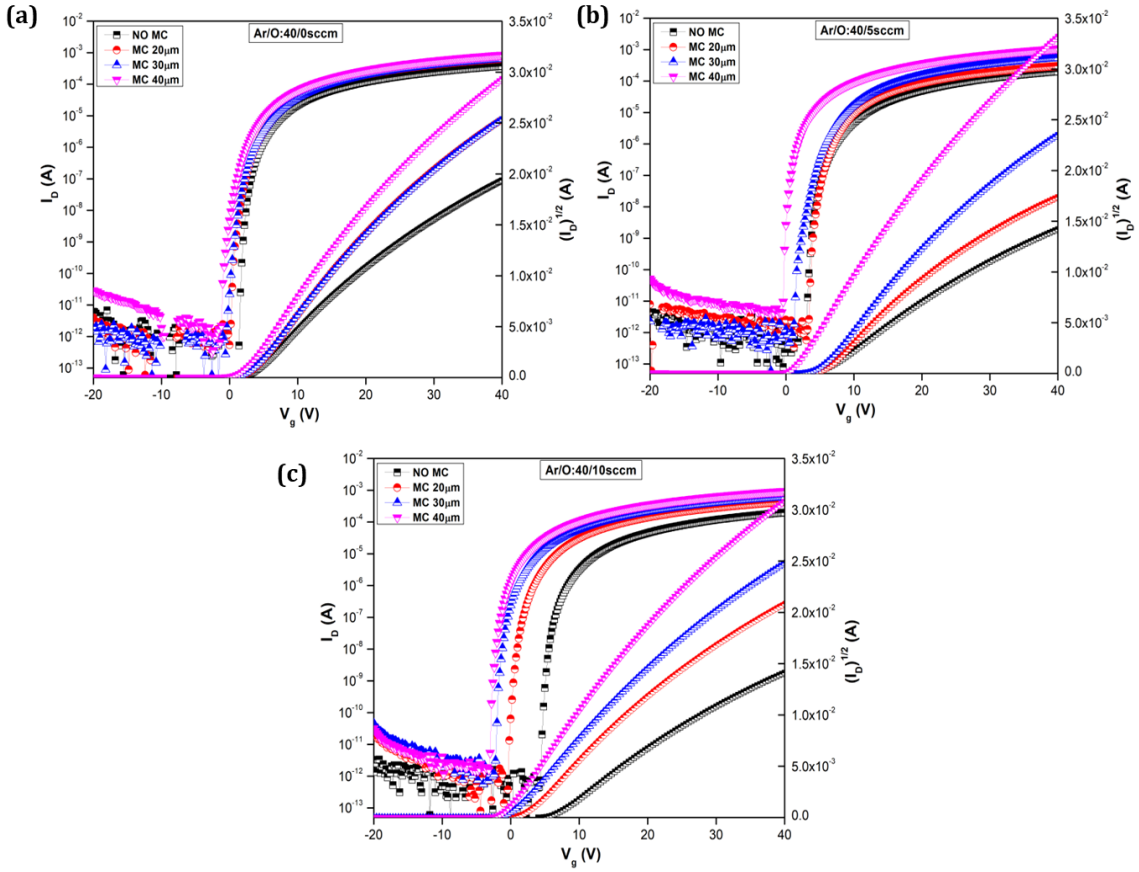

Figure 2. Transfer curve for different MC width (0, 10, 20 and 30μm) with different Oxygen partial pressures **(a)** 0, **(b)** 5 and **(c)** 10sccm at VD = 5.1V

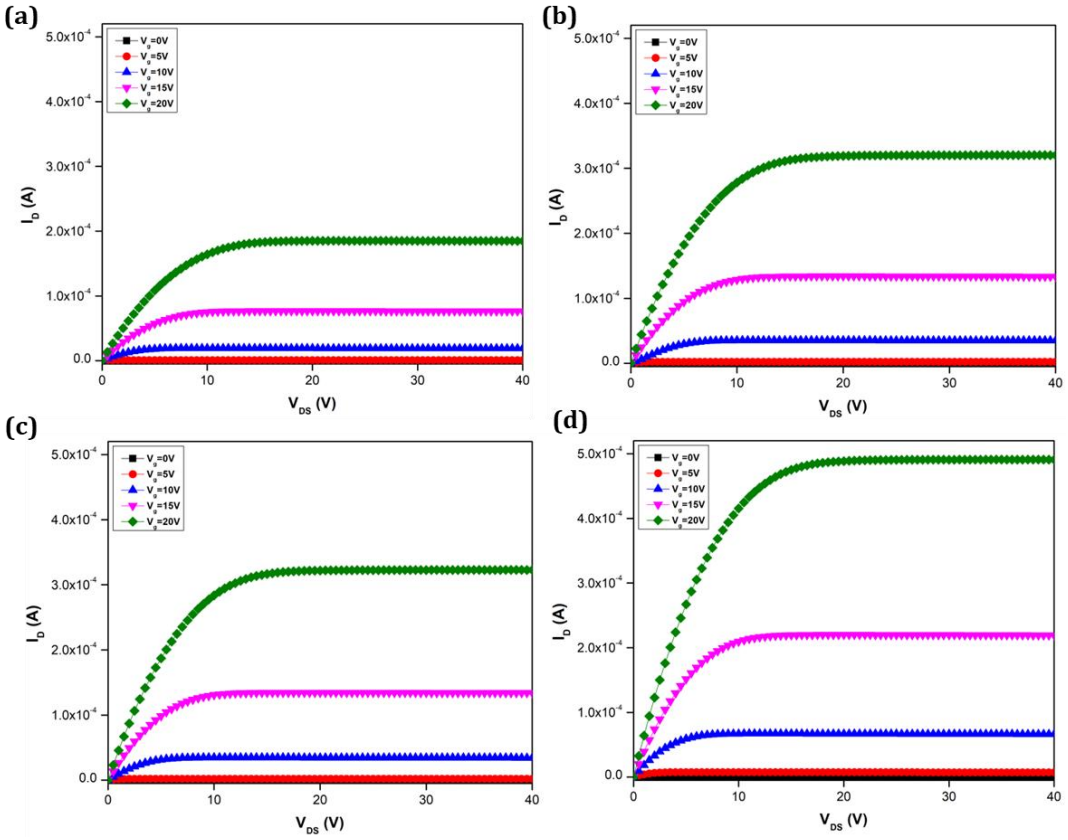

Figure 3. Output characteristics of Metal capped SZTO TFTs for different MC width of **(a)** 0, **(b)** 20, **(c)** 30 and **(d)** 40μm, without OFP

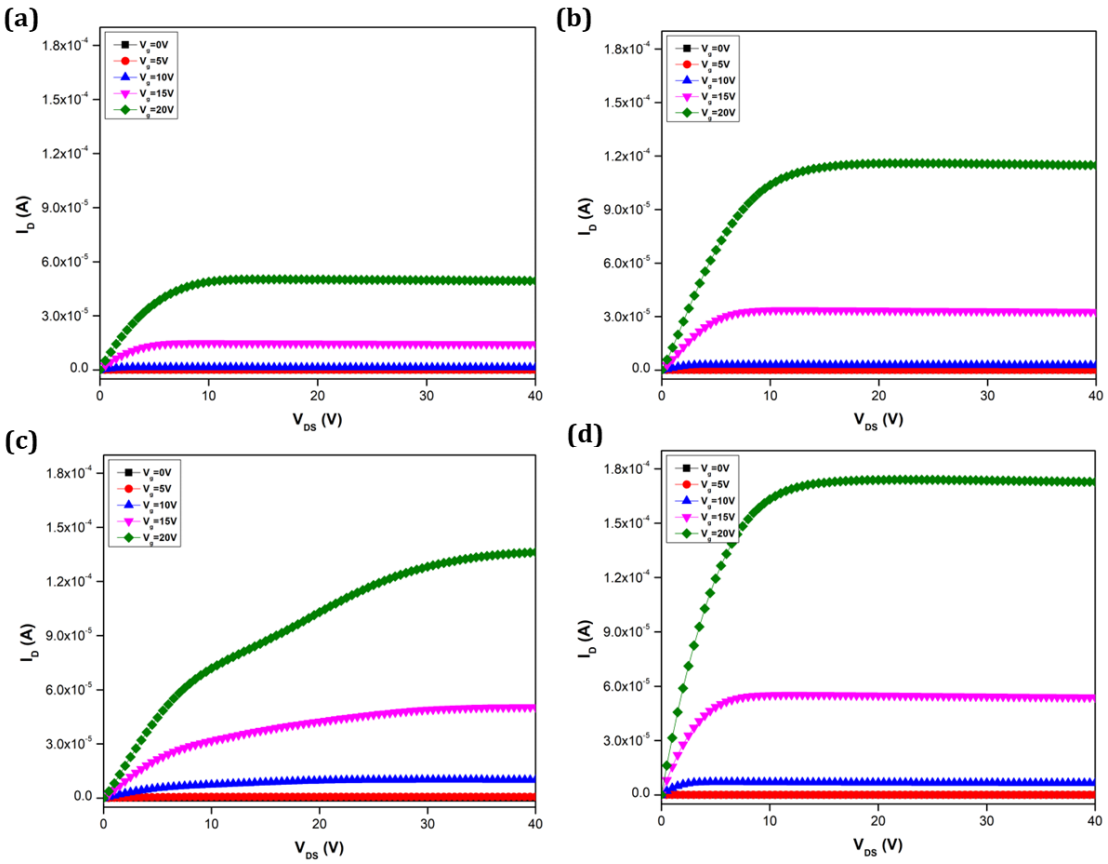

Figure 4. Output characteristics of Metal capped SZTO TFTs for different MC width of **(a)** no MC, **(b)** 20µm, **(c)** 30µm and **(d)** 40µm, with OFP of 10sccm.

The influence of the capping layer is also clearly reflected in the results of the key electrical parameters. These changes indicate that the metal capping layer not only enhances electron transport in the channel but also improves switching characteristics by reducing the voltage required for channel formation. The improved mobility may be related to the higher effective electron density and reduced transport limitation in the capped devices, while the reduction in SS suggests improved switching efficiency and a possible decrease in interfacial trap influence during operation [2].

Generally, the results indicate that OFP and MC width act in opposite ways on TFT operation. Increasing OFP tends to suppress defects and improve switching behavior, but it reduces mobility and shifts V_{th} positively because of lower carrier density. In contrast, increasing MC width enhances electron transport and shifts V_{th} negatively because of electron injection from the capping layer, but it can worsen SS and increase N_T. Therefore, device performance must be optimized by balancing the oxygen content and capping geometry. Among the tested conditions, wider metal capping is particularly effective for compensating the mobility loss caused by oxygen-rich deposition, although too much capping may lead to increased trap-related degradation [2, 28].

These results are in good agreement with the output characteristics of the fabricated TFTs as shown Figure 3 and 4. The enhancement in drain current seen in the output curves corresponds well with the increase in μ_{FE} and the negative shift in V_{th} observed in the transfer characteristics after introducing the metal capping layer. As the capping width increases, electron injections from the Ti/Al capping layer into the a-SZTO channel enhances channel conductivity, resulting in higher current driving capability. In contrast, devices fabricated at higher oxygen flow rates exhibit relatively reduced drain current in the output characteristics, which is consistent with the lower mobility and positive threshold voltage shift caused by reduced oxygen-vacancy-related donor states. Therefore, the trends observed in both transfer and output measurements are mutually consistent, confirming that oxygen flow and metal capping width play decisive roles in modulating the electrical behavior of a-SZTO TFTs.

4. Conclusion

The electrical characteristics of a-SZTO TFTs were successfully tuned by controlling the oxygen flow

parameter during channel deposition and the metal capping width. Increasing the OFP improved the switching characteristics by reducing SS and N_T, indicating suppression of oxygen-vacancy-related defects and a lower density of trap states. However, this also reduced the field-effect mobility and shifted the threshold voltage toward the positive direction because of the decreased free carrier concentration in the a-SZTO channel. On the other hand, the introduction of the Ti/Al metal capping layer significantly enhanced charge transport, increased μ_{FE}, and shifted V_{th} toward the negative region due to electron injection from the capping layer into the semiconductor channel. The improvement observed in the extracted parameters was also well supported by the output characteristics, which showed higher drain current and enhanced channel conduction for capped devices. Although wider metal capping improved current transport, it also caused an increase in SS and N_T at higher widths, suggesting a trade-off between enhanced electron injection and additional trap-related effects. Overall, the results confirm that OFP and MC width are two key parameters for modulating the electrical performance of a-SZTO TFTs. A proper balance between oxygen incorporation and capping geometry is therefore essential for achieving improved mobility, controlled threshold voltage, and better device stability. This study provides useful insight into the design of high-performance a-SZTO TFTs for next-generation flat panel display applications.

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Author Contribution Statement

Balaji Murugan: Conceptualization, Methodology, Validation, Investigation, Writing-Original Draft, Visualization. Author Read and Approved the Final Version of Manuscript.

Does this article screened for similarity?

Yes

Conflict of interest

The Author declares that there is no conflict of interest anywhere.

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